CLAIMS

1. A data processing system, comprising:

a power management unit;

a first processor coupled to said power management unit;

a voltage control module coupled to said power management unit and said first processor for selecting a first voltage level, said voltage control module providing a first control signal and a second control signal to indicate said first voltage level to said power management unit, said power management unit providing a first supply voltage corresponding to said first voltage level to said first processor in response to receiving said first control signal and said first standby signal.

2. The data processing system of claim 1, wherein said first processor provides a first voltage level request to said voltage control module.

3. The data processing system of claim 2, wherein said first processor provides a first sleep mode indicator to said voltage control module, wherein said first control signal is based on said first voltage level request and said first sleep mode indicator, and said second control signal is based on said first sleep mode indicator.

4. The data processing system of claim 3, further comprises control storage circuitry which stores the first voltage level request from said first processor.

5. The data processing system of claim 3, further comprising a second processor which provides a second voltage level request and a second sleep mode indicator to said voltage control module.

6. The data processing system of claim 5, wherein said first control signal is based on said first voltage level request, said first sleep mode indicator, said second voltage level request, and said second sleep mode indicator, and wherein said second control signal is based on said first sleep mode indicator and said second sleep mode indicator.

7. The data processing system of claim 6, wherein said power management unit comprises a regulator, said regulator providing said first supply voltage to said first processor and said second processor.

8. The data processing system of claim 5, wherein said voltage control module selects a second voltage level and provides a third control signal and a fourth control signal to indicate said second voltage level to said power management unit, said power management unit providing a second supply voltage corresponding to said second voltage level to said second processor in response to receiving said third control signal and said fourth control signal.

9. The data processing system of claim 8, wherein said power management unit comprises a first regulator and a second regulator, said first regulator

providing said first supply voltage to said first processor and said second regulator providing said second supply voltage to said second processor.

10. A data processing system, comprising:

a first processor;

a voltage control module coupled to said first processor, wherein said voltage control module receives at least one desired voltage level indicator from said first processor and, based on the at least one desired voltage level indicator from said first processor, provides a first control signal and a second control signal indicating a first supply voltage level to be provided to the first processor.

11. The data processing system of claim 10, wherein the at least one desired voltage level indicator from said first processor comprises a first sleep mode indicator and a first requested voltage level provided by the first processor.

12. The data processing system of claim 11, wherein said first control signal is based on said first sleep mode indicator and said first requested voltage level, and said second control signal is based on said first sleep mode indicator.

13. The data processing system of claim 12, further comprising a voltage regulator which provides said first supply voltage to said first processor.

14. The data processing system of claim 13, wherein said voltage regulator is capable of being optimized based on at least one of said first control signal and said second control signal.

15. The data processing system of claim 11, further comprising control storage circuitry which stores said first requested voltage level

16. The data processing system of claim 10, further comprising:
a second processor, wherein said voltage control module is coupled to said second processor and wherein said voltage control module receives at least one desired voltage level indicator from said second processor, wherein:
said at least one desired voltage level indicator from said first processor comprises a first sleep mode indicator and a first requested voltage level provided by said first processor,
said at least one desired voltage level indicator from said second processor comprises a second sleep mode indicator and a second requested voltage level provided by said second processor.

17. The data processing system of claim 16, wherein said first control signal is based on said first sleep mode indicator, said second sleep mode indicator, said first requested voltage level, and said second requested voltage level, and wherein said second control signal is based on said first sleep mode indicator and said second sleep mode indicator.

18. The data processing system of claim 17, further comprising a voltage regulator which provides said first supply voltage level to said first processor and to said second processor.

19. The data processing system of claim 18, wherein said voltage regulator is capable of being optimized based on at least one of said first control signal, and said second control signal.

20. The data processing system of claim 16, wherein said voltage control module provides a third control signal and a fourth control signal indicating a second supply voltage level to be provided to the second processor, wherein:.

said first control signal is based on said first sleep mode indicator and said first requested voltage level,

said second control signal is based on said first sleep mode indicator;

said third control signal is based on said second sleep mode indicator and said second requested voltage level, and

said fourth control signal is based on said first sleep mode indicator.

21. The data processing system of claim 20, further comprising a first voltage regulator which provides said first supply voltage level to said first processor and a second voltage regulator which provides said second supply voltage level to said processor.

22. The data processing system of claim 21, wherein said first voltage regulator is optimizable based on at least one of said first control signal, said second

control signal, said third control signal, and said fourth control signal, and said second voltage regulator is optimizable based on at least one of said first control signal, said second control signal, said third control signal, and said fourth control signal.

23. A method of generating supply voltage in a data processing system having a first processor, comprising:

receiving a first sleep mode indicator from said first processor;

receiving a first voltage level indicator indicating a first voltage level;

providing a first standby signal based on said first sleep mode indicator;

providing a first control signal based on said first voltage level indicator and said first sleep mode indicator; and

providing a first supply voltage to said first processor based on said first control signal and said first standby signal.

24. The method of claim 23, wherein said first supply voltage has a voltage level different from said first voltage level.

25. The method of claim 23, wherein the data processing system further comprises a second processor, said method further comprising:

receiving a second sleep mode indicator from said second processor;

receiving a second voltage indicator indicating a second voltage level;

providing a second standby signal based on said second sleep mode indicator;

26. The method of claim 25, further comprising:

providing a second control signal based on said second voltage indicator and said second sleep mode indicator;

providing a second standby signal based on said second sleep mode indicator; and

providing a second supply voltage to said second processor based on said second control signal and said second standby signal.

27. The method of claim 25, wherein:

said first standby signal is based on said first sleep mode indicator and said second sleep mode indicator,

said first control signal is based on said first voltage level indicator, said first sleep mode indicator, said second voltage level indicator, and said second sleep mode indicator, and

said first supply voltage is provided to said first processor and said second processor.